

Claims

I claim:

- 5 1. A programmable logic device (PLD), comprising:

 a memory controller, comprising:

 a first controller, the first controller configured to communicate via a

 shared interface with a first memory external to the programmable

 logic device (PLD);

10 a second controller, the second controller configured to communicate via

 the shared interface with a second memory external to the

 programmable logic device (PLD); and

 an arbitration circuitry, the arbitration circuitry configured to arbitrate

 ownership of the shared interface by the first and second

15 controllers.

2. The programmable logic device (PLD) according to claim 1, wherein the shared

interface comprises an address signal, a data signal and a control signal.

3. The programmable logic device (PLD) according to claim 2, wherein the arbitration circuitry communicates with the first controller via a first signal link, and wherein the arbitration circuitry communicates with the second controller via a second signal link.
- 5 4. The programmable logic device (PLD) according to claim 3, wherein the second signal link includes at least one status signal and at least one control signal.
5. The programmable logic device (PLD) according to claim 4, wherein the data signal in the shared interface comprises a write data signal.
6. The programmable logic device (PLD) according to claim 5, further comprising:
10 a first signal selector, the first signal selector configured to receive a first address signal from the first controller and a second address signal from the second controller, the first signal selector further configured to selectably provide as the address signal one of the first and second address signals;
15 a second signal selector, the second signal selector configured to receive a first write data signal from the first controller and a second write

data signal from the second controller, the first signal selector further configured to selectably provide as the write data signal one of the first and second write data signals.

7. The programmable logic device (PLD) according to claim 6, further comprising a
5 third signal selector, the third signal selector configured to receive a first control signal from the first controller and a second control signal from the second controller, the third signal selector further configured to selectably provide as the control signal one of the first and second control signals.

8. The programmable logic device (PLD) according to claim 7, wherein the control
10 signal comprises an output-enable signal.

9. The programmable logic device (PLD) according to claim 4, wherein the at least one status signal in the second data link comprises a request signal, and wherein the second controller uses the request signal to request ownership of the shared interface.

10. The programmable logic device (PLD) according to claim 9, wherein the at least
15 one control signal in the second data link comprises a grant signal, and wherein the

arbitration circuitry uses the grant signal to grant ownership of the shared interface to the second controller.

11. The programmable logic device (PLD) according to claim 10, wherein the at least one control signal in the second data link further comprises a release signal, and wherein
5 the arbitration circuitry uses the release signal to cause the second controller to relinquish ownership of the shared interface.

12. A data-processing system, comprising:
a programmable logic device (PLD), comprising:
a first memory controller, the first memory controller coupled to a first
10 memory external to the programmable logic device (PLD);
a second memory controller, the second memory controller coupled to a
second memory external to the programmable logic device (PLD);
and
a configurable memory interface, the configurable memory interface
15 adapted to selectably provide a shared memory interface
configured to provide communication between the first and second
controllers and the respective first and second memories.

13. The data-processing system according to claim 12, wherein the configurable memory interface provides a shared memory interface in response to a first state of a share-control signal.

14. The data-processing system according to claim 13, wherein the shared memory
5 interface comprises an address signal, a data signal and a control signal.

15. The data-processing system according to claim 14, wherein the configurable memory interface selectably provides as the address signal of the shared interface one of first and second address signals received from the first and second memory controllers, respectively; and wherein the configurable memory interface selectably provides as the
10 data signal of the shared interface one of first and second write data signals received from the first and second memory controllers, respectively.

16. The data-processing system according to claim 15, wherein the configurable memory interface selectably provides as the control signal of the shared interface one of first and second output-enable signals received from the first and second memory
15 controllers, respectively.

17. The data-processing system according to claim 16, wherein the configurable memory interface arbitrates communication between first and second controllers and the first and second memories, respectively.
18. The data-processing system according to claim 17, wherein the configurable
5 memory interface uses a priority arbitration scheme.
19. The data-processing system according to claim 17, wherein the configurable memory interface uses a round-robin arbitration scheme.
20. The data-processing system according to claim 19, wherein the first memory comprises a dynamic random-access memory (DRAM).
- 10 21. The data-processing system according to claim 20, wherein the configurable memory interface is further configured to arbitrate communication between first and second controllers and the first and second memories, respectively, so as to accommodate refreshing the dynamic random-access memory (DRAM).

22. The data-processing system according to claim 21, wherein the first memory comprises a synchronous dynamic random-access memory (SDRAM).
23. The data-processing system according to claim 13, wherein the configurable memory interface provides a non-shared memory interface in response to a second state
5 of the share-control signal.
24. The data-processing system according to claim 23, wherein the shared memory interface further comprises a read data signal, and wherein the configurable memory interface is further configured to selectably provide the read data signal to the second memory controller.
- 10 25. The data-processing system according to claim 12, wherein the programmable logic device (PLD) further comprises a processor.
26. The data-processing system according to claim 25, wherein the processor couples to the first memory.

27. The data-processing system according to claim 25, wherein the processor couples to the second memory.
28. The data-processing system according to claim 22, wherein the second memory comprises a read-only memory (ROM).
- 5 29. The data-processing system according to claim 22, wherein the second memory comprises a programmable read-only memory (PROM).
30. The data-processing system according to claim 22, wherein the second memory comprises an erasable programmable read-only memory (EPROM).
31. The data-processing system according to claim 22, wherein the second memory
10 comprises a FLASH memory.
32. A method of processing information using a programmable logic device (PLD), the method comprising:

communicating via a shared interface with a first memory, the first memory being
external to the programmable logic device (PLD);

communicating via the shared interface with a second memory, the second
memory being external to the programmable logic device (PLD); and

5 arbitrating ownership of the shared interface by the first and second controllers.

33. The method according to claim 32, further comprising communicating via the
shared interface an address signal, a data signal and a control signal.

34. The method according to claim 33, wherein communicating via the shared
interface with the first memory further comprises communicating via a first signal link,
10 and wherein communicating via the shared interface with the second memory further
comprises communicating via a second signal link.

35. The method according to claim 34, wherein communicating via the second signal
link further comprises communicating via at least one status signal and at least one
control signal.

36. The method according to claim 35, wherein the data signal in the shared interface comprises a write data signal.

37. The method according to claim 36, further comprising:

receiving a first address signal from the first controller and a second

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address signal from the second controller;

selectably providing as the address signal one of the first and second

address signals;

receiving a first write data signal from the first controller and a second

write data signal from the second controller; and

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selectably providing as the write data signal one of the first and second

write data signals.

38. The method according to claim 37, further comprising:

receiving a first control signal from the first controller and a second

control signal from the second controller; and

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selectably providing as the control signal one of the first and second

control signals.

39. The method according to claim 38, wherein the control signal comprises an output-enable signal.
40. The method according to claim 35, wherein the at least one status signal in the second data link comprises a request signal, the method further comprising using, by the
5 second controller, the request signal to request ownership of the shared interface.
41. The method according to claim 40, wherein the at least one control signal in the second data link comprises a grant signal, the method further comprising using the grant signal to grant ownership of the shared interface to the second controller.
42. The method according to claim 41, wherein the at least one control signal in the
10 second data link further comprises a release signal, the method further comprising using the release signal to cause the second controller to relinquish ownership of the shared interface.